DERWENT-ACC-NO: 2002-477755

DERWENT-WEEK: 200251

TITLE: Capacitor formation of semiconductor device

INVENTOR: KWON, O S

PATENT-ASSIGNEE: HYNIX SEMICONDUCTOR INC[HYNIN]

PRIORITY-DATA: 2000KR-0036859 (June 30, 2000)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 2002002633 A	January 10, 2002	N/A	001	H01L 021/8242

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR2002002633A	N/A	2000KR-0036859	June 30, 2000

INT-CL (IPC): H01L021/8242

ABSTRACTED-PUB-NO: KR2002002633A

BASIC-ABSTRACT:

NOVELTY - A method for forming a capacitor of a semiconductor device is provided to easily enable high integration, by easily using a (Ba,Sr)TiO3(BST) dielectric layer used in a design rule not greater than 0.1 micrometer.

DETAILED DESCRIPTION - A **Pt seed** layer(25) is formed on a lower insulation layer(21) having a contact plug(23), and an oxide layer is formed on the **Pt seed** layer. A stacked structure of the **Pt seed** layer remaining in the upper portion of a storage electrode contact region and an oxide layer pattern is formed. A nitride layer is formed on the resultant structure including the

oxide layer pattern. A photoresist layer filling the gap between the oxide layer patterns is formed. The photoresist layer and the nitride layer are etched to expose the oxide layer pattern by a planarization etch process. The oxide layer pattern is removed by using a buffered oxide etchant(BOE) solution to expose the **Pt seed** layer. A Pt layer(33) filling the gap between the photoresist layers is formed on the **Pt seed** layer by an ion plating process. The nitride layer is eliminated to form a Pt storage electrode coupled to the storage electrode contact plug.

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS: CAPACITOR FORMATION SEMICONDUCTOR DEVICE

DERWENT-CLASS: L03 U11

CPI-CODES: L04-C14A;

EPI-CODES: U11-C05G1B; U11-C18B5;

SECONDARY-ACC-NO:
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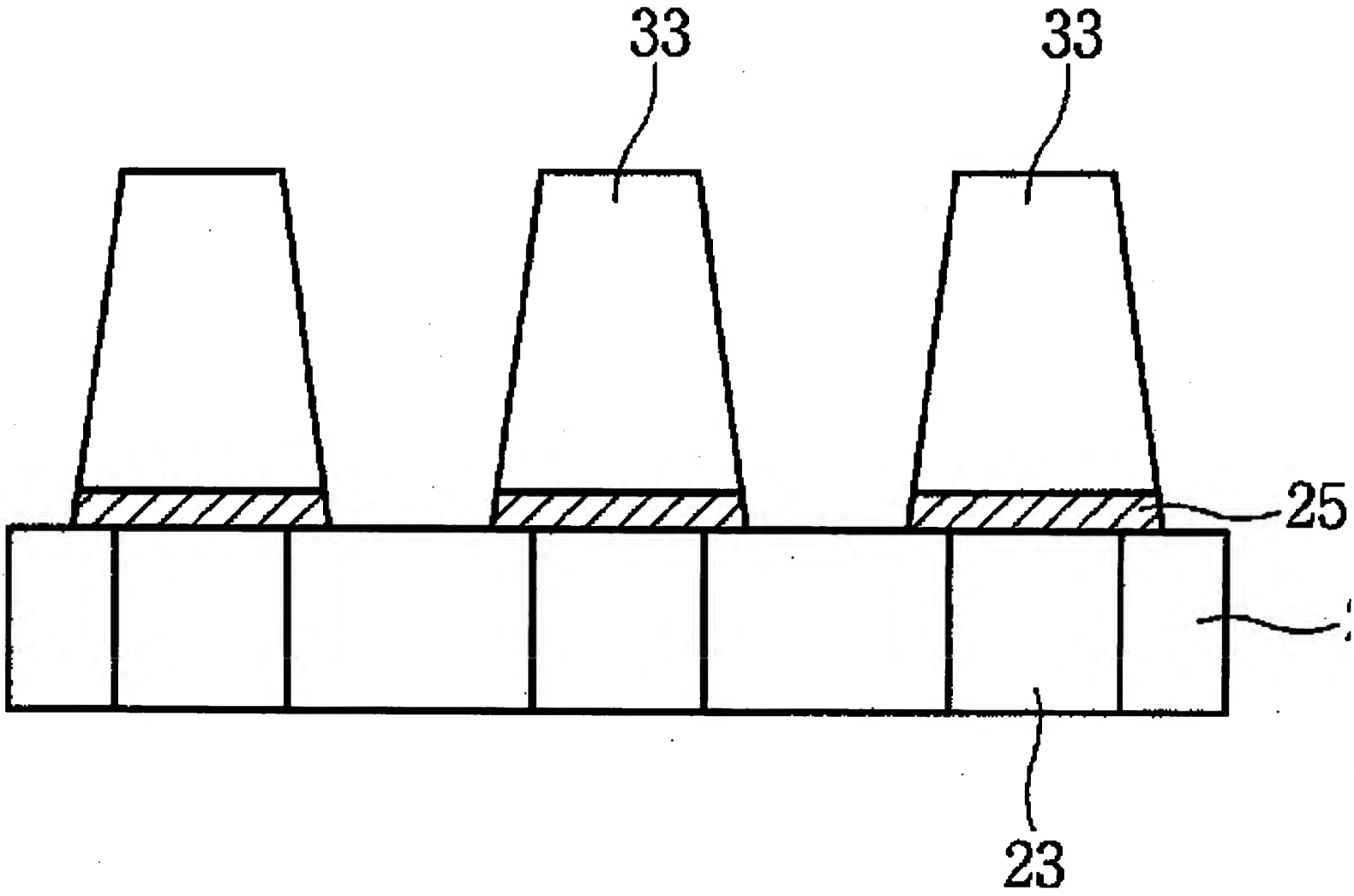
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